CLAIMS

1. An insulated gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising:

a semiconductor body layer (10);

a source electrode (22) extending across a source region of the semiconductor body layer (10) defining a Schottky potential barrier between the source electrode (22) and the source region (32) of the semiconductor body layer,

a drain electrode (24) connected to the semiconductor body layer; and

a gate electrode (4) for controlling transport of carriers of the predetermined carrier type from the source electrode (22) to the source region (32) of the semiconductor body layer (10) across the barrier when the source region is depleted;

wherein the gate electrode (4) is arranged in an overlapping relationship to the source electrode on the opposite side of the semiconductor body layer to the source electrode having a gate insulator layer (8) between the gate electrode and the semiconductor body layer; and

the gate electrode (4) is spaced from the source electrode (22) by at least the combined full thickness of the semiconductor body layer (10) and the gate insulator (8) over the whole of the gate-controlled region of the Schottky barrier.

2. An insulated gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising:

a semiconductor body layer (10) having a thickness of at least 10 nm;

a source electrode (22) extending across a source region of the semiconductor body layer (10) defining a potential barrier between the source electrode (22) and a source region (32) of the semiconductor body layer,

a drain electrode (24) connected to the semiconductor body layer; and

a gate electrode (4) for controlling transport of carriers of the predetermined carrier type from the source electrode (22) to the source region

(32) of the semiconductor body layer (10) across the barrier when the source region is depleted;

wherein the gate electrode (4) is arranged in an overlapping relationship to the source electrode on the opposite side of the semiconductor body layer to the source electrode having a gate insulator layer (8) between the gate electrode and the semiconductor body layer; and

the gate electrode (4) is spaced from the source electrode by at least the combined thickness of the full thickness of the semiconductor body layer (10) and the gate insulator (8) over the whole of the gate-controlled region of the source barrier.

3. A transistor according to any preceding claim including dopant impurities in the semiconductor body layer under the source electrode for controlling the effective barrier height.

4. A transistor according to claim 3 wherein the dopant is a shallow implant of donor impurities to raise the effective barrier height to holes and to lower the effective barrier height to electrons.

5. A transistor according to any preceding claim further comprising a field relief structure (42, 44, 38, 71) at the lateral edge of the source electrode facing the drain electrode.

6. A transistor according to claim 5 wherein the drain electrode (24) is connected to a drain region (36) of the semiconductor body layer (10), the drain region (36) being spaced from the source region (32) by an intermediate region (34) of the semiconductor body layer (10), and

the field relief structure is the intermediate region (34) of the semiconductor body layer between the source region (32) and the drain region (36), the intermediate region being compensated.

7. A transistor according to claim 5 wherein the drain electrode (24) is connected to a drain region (36) of the semiconductor body layer (10), the drain region (36) being spaced from the source region (32) by an intermediate region (34) of the semiconductor body layer (10), and

the field relief structure comprises an extension (44) to the source electrode extending laterally across at least part of the intermediate region (34), separated from the said part of the intermediate region by a field relief insulating layer (42).

8. A transistor according to any preceding claim wherein the the drain electrode (24) is connected to a drain region (36) of the semiconductor body layer (10), the drain region (36) being spaced from the source region (32) by an intermediate region (34) of the semiconductor body layer (10), and

the lateral extent of the intermediate region (34) between the drain region and the source region is less than 5 micrometer.

9. A transistor according to any preceding claim wherein the lateral extent of the gate electrode (4) towards the drain is overlapped wholly by the source electrode (22).

10. A transistor according to any preceding claim comprising a pair of drain electrodes (24) and corresponding drain regions (36) of the semiconductor body layer (10) laterally on either side of the source region (32).

11. A transistor according to any preceding claim wherein the potential barrier has a barrier potential for the predetermined charge carrier type of between 0.25 times and 0.75 times the band gap of the semiconductor of the semiconductor body layer.

12. A transistor according to claim 2 further comprising a heterojunction layer (82) between the source electrode and the semiconductor body layer forming the barrier.

13. A transistor according to any preceding claim wherein the semiconductor body layer (10) is a thin film of deposited semiconductor material .

14. A transistor according to any preceding claim wherein the semiconductor body layer (10) is of amorphous silicon.

15. A transistor according to any of claims 1 to 13 wherein the semiconductor body layer (10) is of polysilicon.

16. A transistor according to any of claims 1 to 13 wherein the semiconductor body layer (10) is of organic semiconductor.

17. An insulated gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising:

a semiconductor body layer;

a laterally-extending source electrode defining a lateral barrier at one major side of the semiconductor body layer;

a drain electrode laterally spaced along the semiconductor body layer from the source electrode by an intermediate region of the semiconductor body layer;

a gate electrode extending laterally on the opposite major side of the semiconductor body layer to the source electrode to define a gate-controlled region of the semiconductor body layer extending across the semiconductor body layer to the source barrier;

a gate insulator layer between the gate electrode and the semiconductor body layer; and

a field relief structure on the edge of the source region facing the drain region.

18. An insulated-gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising:

a semiconductor layer that provides a body portion of the transistor between a source of the said carriers and a drain for the said carriers; and

an insulated gate including a gate electrode coupled to the body portion via an intermediate gate-dielectric layer;

wherein

the source comprises a barrier to the said carriers between a source electrode and the semiconductor layer so as to inhibit carrier flow from the source into the body portion except as controlled by the insulated gate;

the source and the insulated gate are located at respective opposite major sides of the semiconductor layer in an opposed laterally-overlapping relationship which separates the source from the insulated gate by at least an intermediate thickness of the semiconductor layer;

and the laterally-overlapping insulated gate is coupled to the source barrier via the intermediate thickness of the semiconductor layer so as to permit transistor conduction by controlled emission of said carriers across the source barrier by voltage applied between the gate and source electrodes upon depletion of the body portion across the intermediate thickness of the semiconductor layer from the insulated gate.

19. A transistor comprising a source electrode on the opposite side of a semiconductor body layer to an insulated gate electrode, and a drain electrode connected to the semiconductor body layer, wherein the source electrode has a potential barrier to the semiconductor body layer, and source-drain current is controlled by the gate voltage upon depletion of a region of the semiconductor body layer adjacent to the source barrier by the application of suitable source-drain voltage and gate voltage.

20. Use of a transistor according to any preceding claim, including

applying a voltage between the source, gate and drain electrode to substantially deplete the whole of the source region (22) of the semiconductor

body layer in the region of the gate electrode and to cause carriers of the predetermined conductivity type to be emitted by the source electrode across the barrier and across the depleted source region to the drain region and then to the drain electrode.

21. Use of a transistor according to any claim 20 including varying the source-gate voltage to vary the source-drain current.

22. A transistor arrangement, comprising

a substrate (2); and

a plurality of transistors according to any of claims 1 to 19 distributed over the substrate.

23. A transistor arrangement according to claim 22 including both n-type and p-type transistors according to any of claims 1 to 19.

24. A transistor arrangement according to claim 23 wherein there is a shallow implant of donor impurities under the barriers of p-type and n-type transistors to raise the effective barrier height to holes in the p-type transistors and to lower the effective barrier height to electrons in the n-type transistors.

25. A transistor circuit, including

an insulated gate field effect transistor having a semiconductor body layer (10), a source electrode (22) and a gate electrode (4) arranged in opposed relationship on opposite sides of the semiconductor body layer (10), with a barrier between the source electrode and the semiconductor body layer and a gate insulator (8) between the semiconductor body layer and the gate, and a drain electrode (24) connected to the semiconductor body layer (10); and

a circuit (33, 35) arranged to apply voltages to source, gate and drain electrodes to deplete the semiconductor body layer in the region of the source electrode and to control the barrier height of the barrier by the source-gate

voltage to control the emission of carriers from the source electrode to the semiconductor body layer and hence to control the source-drain current by the source-gate voltage.

26. A method of operating a transistor having a source electrode (22), a drain electrode (24), a semiconductor body layer (10) having a source region (32) in contact with the source electrode (22) and a drain region (36) in contact with the drain electrode (24), and an insulated gate (4) opposed to the source electrode (22), the method including:

applying a voltage between the source, gate and drain to substantially deplete the whole of the source region of the semiconductor body layer and to cause carriers to be emitted by the source electrode across the barrier and across the depleted source region to the drain region and then to the drain electrode.

27. A method according to claim 26 including holding the source-drain voltage at a value that depletes the source region and varying the source-gate voltage to control the current flowing from source to drain.